Summary of Background Art

This part of the Formal Replay to the 2nd OA provides the summary of background art communicated by the inventor during earlier prosecution stages, in order to improve visibility of such informations related to the closest background art known.

Closest background art for this invention is represented by the documents listed below:
D1 (US 5,668,830 by Georgiu)
D2 (PCT/CA01/00723 by Bogdan);
D3 (US 2002/0009171 by Ribo);
D4 (US 5,592,125 by Williams);
D5 (US 6,987,817 by Reuveni)

The D1 is limited to using delay lines and most basic digital filters for removing phase noise of waveform edges. D1 circuits enable merely edge phase aligning and data re-timing on a bit per bit basis for data serializing/de-serializing only.
Consequently, D1 circuits do not have any of the fundamental features of the present invention such as; over-sampling and noise filtering from entire pulse necessary for elimination of noise occurring inside data pulses, or cumulative processing operations necessary for measuring and processing lengths of transmitted pulses, or adaptive signal processing using wave-form screening.

The D2 solution created variety of high resolution phase capturing techniques which are useful for measuring phase skews between low frequency frames in high quality synchronization circuits. However these D2 phase capturing techniques have never been targeting any processing throughput which could be even close to that needed for communication signal processing. Therefore besides said high resolution phase capture, the D2 solution has fundamentally different principle of operation and produces entirely different results.

Consequently D2 can not contribute to any processing of much higher frequency signals commonly used in communication links.

The D3 solution represents latest generation of clock and data recovery (CDR) circuits which over-sample in expected transition region in order to achieve some fractional improvements of jitter tolerance.
The D3 captures windows consisting of samples covering entire data bit interval.
Every such window covers single bit interval only and it is captured and processed separately from other windows on a bit interval by bit interval basis without any correlation between data captured in consecutive windows. Such lack of correlation amounts to inability to filter out narrow glitches occurring between windows.
Therefore the D3 windows need to be centered around expected edges of received data bits in order to enable said bit by bit processing without data recovery errors.
Obviously such window centering can only be achieved by phase locking to the received signal.

Other over-sampling solution is the CDR with bang-bang phase detector (CDR with BBPD) represented by D4.
While taking more samples provides D3 with better base for jitter filtering than that of the CDR with BBPD, dynamics of D3 phase locking has to accommodate additional interference caused by said jiter filtering and by further processing of output data providing return reference for the D3 phase locked loop.
Similarly as the D3 and the CDR with BBPD, all other conventional analyzers and receivers of serial data have the same common feature limiting severely their performances; they require phase locking to received signal in order to recover data based on sampling localized in a credible region of the received wave-form.
The phase locking requirement is not only difficult to achieve but furthermore it imposes significant limitations on receiver performances such as those listed below:

- Jitter tolerance is very low outside the bandwidth of receivers PLL while such PLLs bandwidth is usually below 1/10 of the bandwidth of transmitted signals which are the major sources of phase jitter and amplitude noise.

- Such receivers are defenseless against high frequency noise occurring in wave-form regions which can not be filtered out using said localized sampling.
- Such PLL based receivers require significant lock acquisition times before newly established data link becomes operational what is an impediment for all burst types of data links.

Still other over-sampling solution is described in D5 as designed originally for processing serial data streams from a recordable medium like CD or DVD.
Nevertheless some of D5 teachings describe data recovery circuits, which derive number of data bits received in a waveform pulse by dividing a length of the pulse by a bit widths calculated statistically by processing received signal waveforms.
Such pulse lengths is detected originally as a sum of all oversampling sub-clocks occurring during the pulse, and is divided by such statistically calculated bit width later on.
However such detection of the sub-clocks sum and such divisions involving long pulses, limit data rates which D5 solution can be utilized at.
Furthermore limited accuracy of such statistically calculated bit widths and division error accumulated during any long pulse processing, increase error rates and limit reliability.
Still furthermore; since such statistical processing of the bit widths is performed in a closed loop, it can cause stability problems due to highly unpredictable phase noise in the received signal.

It is explained further below that the sequential data recovery presented in this application (SDR) enables major advantages, over data recovery solutions presented in such D1-D5, including:
by >>10 times faster phase/frequency detection and ~10 times (by one order of magnitude) more accurate detection of data carrying phase of received signal;
major improvement of phase jitter tolerance being the major factor improving data rates (or link lengths) on high speed links (where higher data rates decrease time interval unit TIU which the phase jitter is measured against).

Such DSP MSP advantages over conventional solutions result from substantially different principles of operation explained below.

The major elements of DSP MSP are; much faster high resolution measurements of entire pulse lengths of incoming wave-form, and much faster digital processing of these accurate pulse lengths for determining data content transmitted by the wave-form.

Since every edge detection provides exact re-timing of the whole received signal, such pulse lengths processing obviously never needs any phase locking.

Furthermore without any phase locking, based on an inexpensive local clock having frequency accuracy +/-30ppm, this invention provides phase jitter tolerance improvements over prior art including: over 6 times better tolerance in a lower 1/3 of received signal bandwidth, and over 2 times better tolerance in the remaining upper 2/3.

Furthermore; since entire received wave-form is uniformly densely sampled and continuously filtered and processed, short glitches caused by high frequency amplitude noise are identified and filtered out before any detection of a valid edge takes place.

Since said exact re-timing is provided by every edge detection this invention solution locks instantly and never requires any acquisition time what makes it ideal for all the burst type communication links.